



501.43323X00

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: A. NISHIDA, et al.  
Application No.: 10/781,861  
Filed: February 20, 2004  
For: A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE  
AND A METHOD OF MANUFACTURING THE SAME  
Art Unit: Unknown  
Examiner: Unknown

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR §§ 1.97 & 1.98**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

April 1, 2003

Sir:

This Information Disclosure Statement is being submitted within three months of the filing date of the above-identified application.

Each of the documents listed on the attached form PTO/SB/08A is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Docket No. 501.43323X00) please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

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PTO/SB/08A (10-01)

Approved for use through 10/31/2002. OMB 0651-0031

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		Application Number	10/781,861		
		Filing Date	February 20, 2004		
		First Named Inventor	A. NISHIDA, et al.		
		Art Unit	Unknown		
		Examiner Name	Unknown		
Sheet	1	of	1	Attorney Docket Number	501.43323X00

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)				

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)					

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS			
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		Shigeyoshi Watanabe, et al., "A Novel Circuit Technology With Surrounding Gate Transistors (SGT's) For Ultra High Density DRAMS's"; IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995, pp 960-971	

Examiner Signature		Date Considered	
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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